IN THE CLAIMS:

The following is a complete listing of claims in this application.

Claims 1-16 (canceled).

17. (currently amended) A process for forming a substrate to be utilized in microelectronics, nanoelectronics, microtechnology or nanotechnology comprising a support having a thin layer formed on an upper surface thereof, comprising the steps of:

forming at least one said thin layer on the upper surface of a nanostructured support, and subsequently

treating the nanostructured support to generate internal strains in the support, causing deformation of the support by <u>dilation or contraction</u> at least in the plane of the thin layer, so as to ensure a corresponding deformation of the thin layer and modification of properties of the thin layer.

- 18. (currently amended) The process as claimed in Claim 17, wherein the treating comprises treating the nanostructured support chemically to cause deformation corresponding to dilation or contraction of the nanostructure thereof.
- 19. (previously presented) The process as claimed in Claim 17, wherein the nanostructured support is selected from the group consisting of a metals, semi-conductors and dielectric materials.
- 20. (previously presented) The process as claimed in Claim 17, additionally comprising effecting the epitaxial growth of a crystalline material on the thin layer, after the treating.
- 21. (previously presented) The process as claimed in Claim 20, wherein the thin layer is selected to be capable of possessing a lattice parameter corresponding to a lattice parameter of a crystalline material to be formed by said epitaxial growth.

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- 22. (previously presented) The process as claimed in Claim 21, wherein the thin layer is prestrained.
- 23. (previously presented) The process as claimed in Claim 17, additionally comprising forming on the nanostructured support at least one intermediate layer disposed between the thin layer and the nanostructured support.
- 24. (previously presented) The process as claimed in Claim 20, wherein the crystalline material is semi-conductor or superconductor material.
- 25. (previously presented) The process as claimed in Claim 17, wherein the thin layer is made of a material having piezoelectric properties.
- 26. (previously presented) The process as claimed in Claim 25, additionally comprising performing a lithographic operation on the thin layer to reveal piezoelectric zones.
- 27. (previously presented) The process as claimed in Claim 25, additionally comprising deforming the nanostructured support so that electrical charges appear in the thin layer.